CY7C1386D, CY7C1386F
CY7C1387D, CY7C1387F

18-Mbit (512 K × 36/1 M × 18) Pipelined DCD Sync SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 200, and 167 MHz
- Registered inputs and outputs for pipelined operation
- Optimal for performance (double-cycle deselect)
- Depth expansion without wait state
- 3.3 V core power supply (V_{DD})
- 2.5 V or 3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 2.6 ns (for 250 MHz device)
- Provides high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® Interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- CY7C1386D/CY7C1387D available in JEDEC-standard Pb-free 100-pin TQFP, Pb-free and non Pb-free 165-ball FBGA package. CY7C1386F/CY7C1387F available in Pb-free and non Pb-free 119-ball BGA package
- IEEE 1149.1 JTAG-compatible boundary scan
- ZZ sleep mode option

Functional Description

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F SRAM[1] integrates 512 K × 36/1 M × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}_1$), depth expansion chip enables (CE_2 and $\overline{CE}_3$ [2]), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW}_X$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle.This part supports byte write operations (see on page 4 and Truth Table on page 11 for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed.This feature allows depth expansion without penalizing system performance.

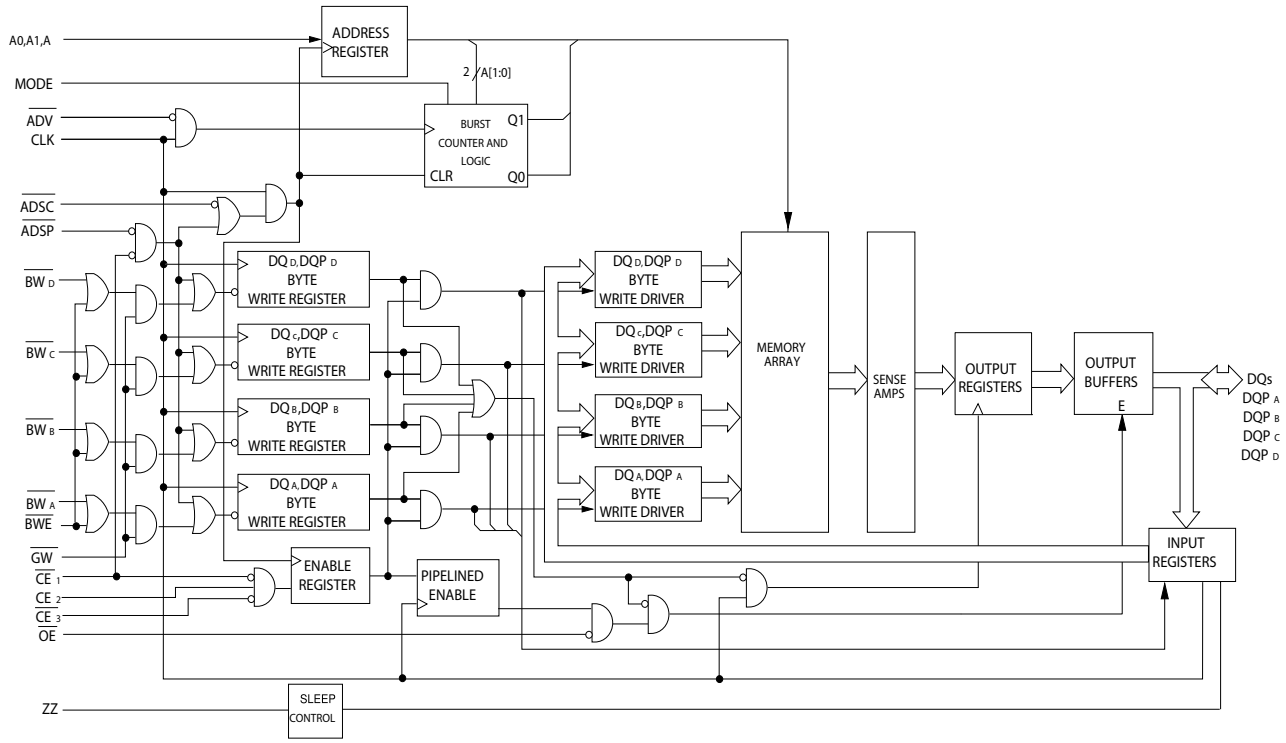
The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F operates from a +3.3 V core power supply while all outputs operate with a +3.3 V or +2.5 V supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

Selection Guide

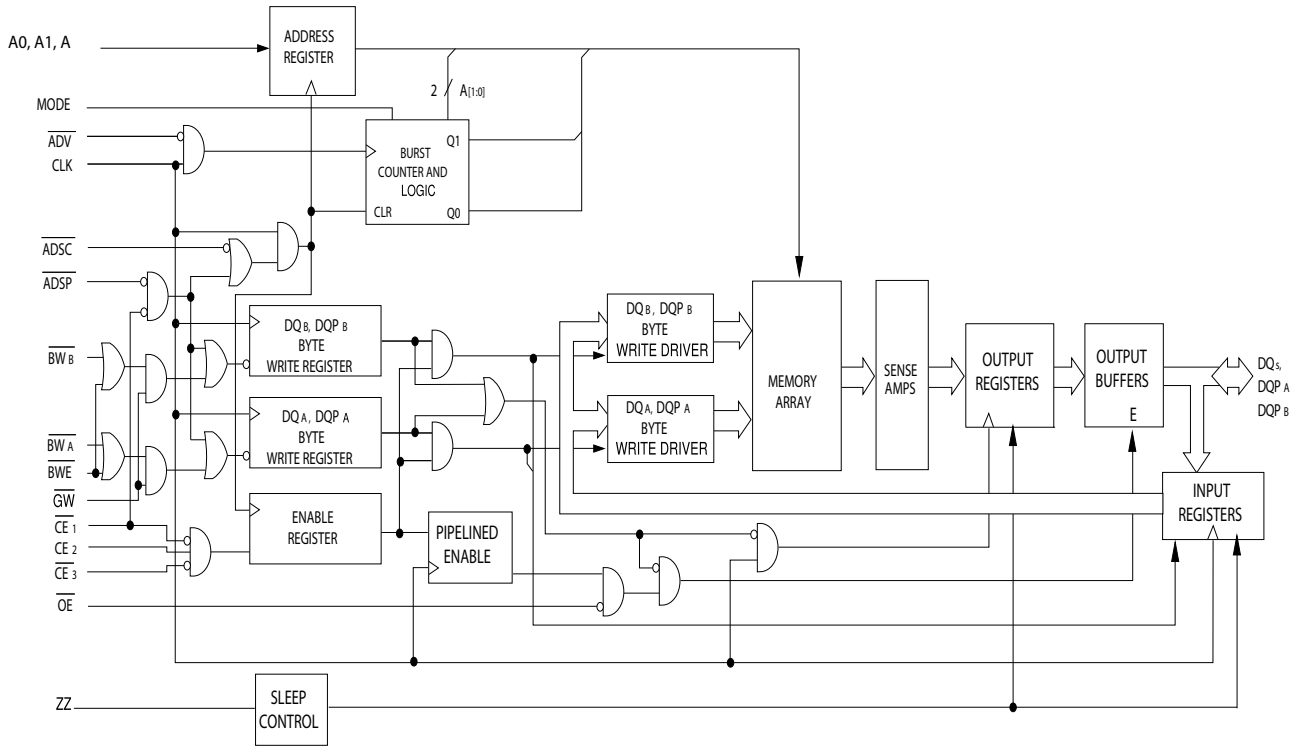
Description	250 MHz	200 MHz	167 MHz	Unit
Maximum access time	2.6	3.0	3.4	ns
Maximum operating current	350	300	275	mA
Maximum CMOS standby current	70	70	70	mA

Notes
1. For best practices or recommendations, please refer to the Cypress application note AN1064, *SRAM System Design Guidelines* on www.cypress.com.
2. $\overline{CE}_3$ and CE_2 are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in Single Chip Enable.

Logic Block Diagram – CY7C1386D/CY7C1386F [3] (512 K × 36)



Logic Block Diagram – CY7C1387D/CY7C1387F [3] (1 M × 18)



Note
3. CY7C1386F and CY7C1387F have only 1 Chip Enable ($\overline{CE}_1$).

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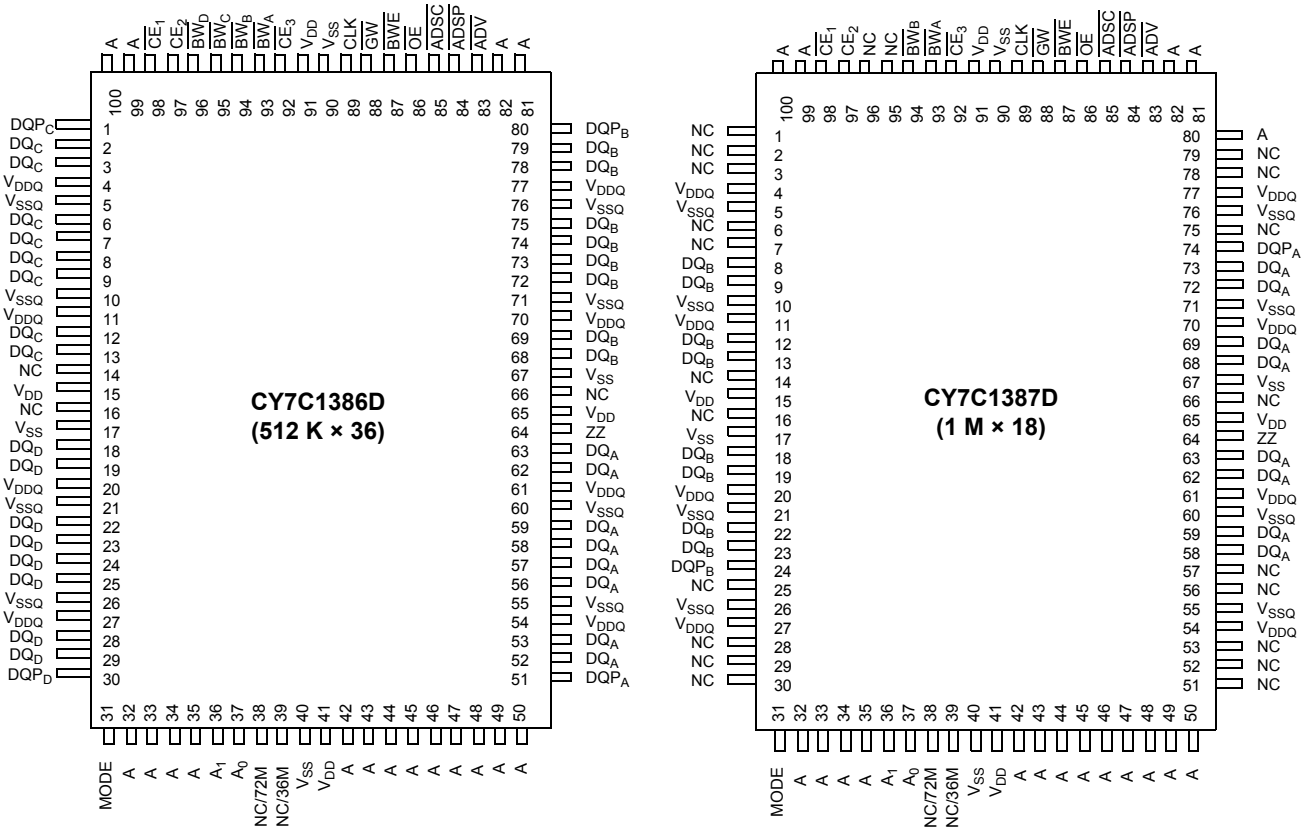
Pin Configurations

Figure 1. 100-pin TQFP (3 Chip Enable)



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Pin Configurations (continued)

Figure 2. 119-ball BGA (1 Chip Enable)

CY7C1386F (512 K × 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	A	A	$\overline{ADSC}$	A	A	NC/576M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW_C}$	$\overline{ADV}$	$\overline{BW_B}$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW_D}$	NC	$\overline{BW_A}$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1387F (1 M × 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	A	A	$\overline{ADSC}$	A	A	NC/576M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{BW_B}$	$\overline{ADV}$	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CLK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	NC	$\overline{BW_A}$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC/72M	A	A	NC/36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

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Pin Configurations (continued)

Figure 3. 165-ball FBGA (3 Chip Enable)

CY7C1386D (512 K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/512M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1387D (1 M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC/144M	A	CE_2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	‘V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

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Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ [4] are sampled active. A1: A0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ [4] to select or deselect the device. $\overline{ADSP}$ is ignored if CE_1 is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2 [4]	Input-Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ [4] to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$ [4]	Input-Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. Not connected for BGA. Where referenced, $\overline{CE}_3$ [4] is assumed active throughout this document for BGA. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, DQ pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ sleep input, active HIGH**. When asserted HIGH places the device in a non-time critical sleep condition with data integrity preserved. For normal operation, this pin has to be LOW. ZZ pin has an internal pull down.
DQs, DQP_X	I/O-Synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tristate condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.

Note
4. $\overline{CE}_3$ and CE_2 are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in Single Chip Enable.

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Pin Definitions (continued)

Name	I/O	Description
MODE	Input-Static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull up.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die.
NC/(36 M, 72 M, 144 M, 288 M, 576 M, 1 G)	–	**These pins are not connected.** They are used for expansion up to 36 M, 72 M, 144 M, 288 M, 576 M, and 1G densities.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium® and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{BWE}$) and byte write select ($\overline{BW_X}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Synchronous chip selects $\overline{CE_1}$, CE_2, $\overline{CE_3}$ [5] and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{CO} if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tristated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported.

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F is a double cycle deselect part. After the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output tristates immediately after the next clock rise.

Note
5. $\overline{CE_3}$ and CE_2 are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in Single Chip Enable.

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Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQ_x inputs is written into the corresponding address location in the memory core. If $\overline{GW}$ is HIGH, the write operation is controlled by $\overline{BWE}$ and $\overline{BW_X}$ signals.

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F provides byte write capability that is described in the write cycle description table. Asserting the byte write enable input ($\overline{BWE}$) with the selected byte write input, selectively writes to the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F is a common I/O device, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. This tristates the output drivers. As a safety precaution, DQ are automatically tristated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQ_X is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F is a common I/O device, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_X inputs. This tristates the output drivers. As a safety precaution, DQ_X are automatically tristated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

[+] Feedback

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq$ V_{DD} – 0.2 V	–	80	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq$ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

[+] Feedback

Truth Table

The Truth Table for CY7C1386D, CY7C1386F, CY7C1387D, and CY7C1387F follow.[6, 7, 8, 9, 10]

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L–H	Tristate
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L–H	Tristate
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L–H	Tristate
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tristate
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tristate
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tristate
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tristate
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
6. X = Do not care, H = Logic HIGH, L = Logic LOW.
7. $\overline{WRITE}$ = L when any one or more byte write enable signals, and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
8. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
9. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. $\overline{OE}$ is a don't care for the remainder of the write cycle.
10. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

[+] Feedback

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1386D and CY7C1386F follows.[11, 12]

Function (CY7C1386D/CY7C1386F)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1387D and CY7C1387F follows.[11, 12]

Function (CY7C1387D/CY7C1387F)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ_A and DQP_A)	H	L	H	L
Write byte B – (DQ_B and DQP_B)	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Notes
11. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
12. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid appropriate write is done based on which byte write is active.

[+] Feedback

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO can be left unconnected. Upon power-up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 15. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The boundary scan order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 18.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in Identification Codes on page 18. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute

[+] Feedback

the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.

IDCODE

The IDCODE instruction causes a vendor specific 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. The SAMPLE Z command places all SRAM outputs into a high Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. As there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required; that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST Output Bus Tristate

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #85 (for 119-ball BGA package) or bit #89 (for 165-ball FBGA package). When this scan cell, called the "extest output bus tristate," is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

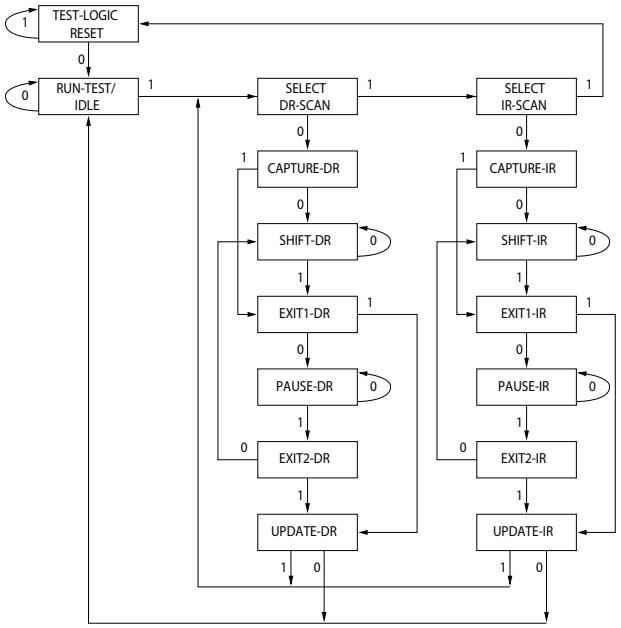
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

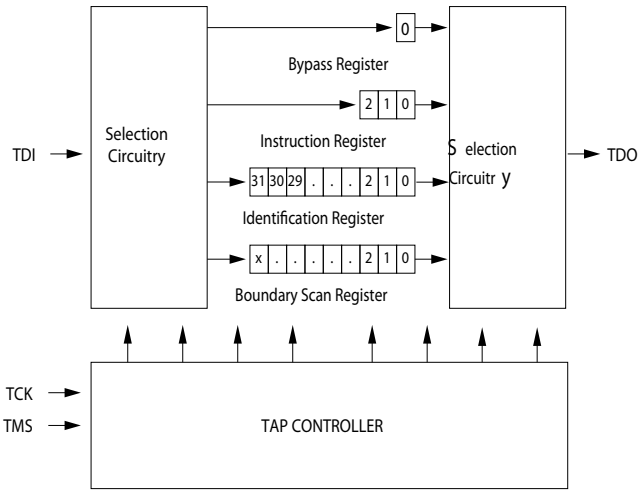
[+] Feedback

TAP Controller State Diagram

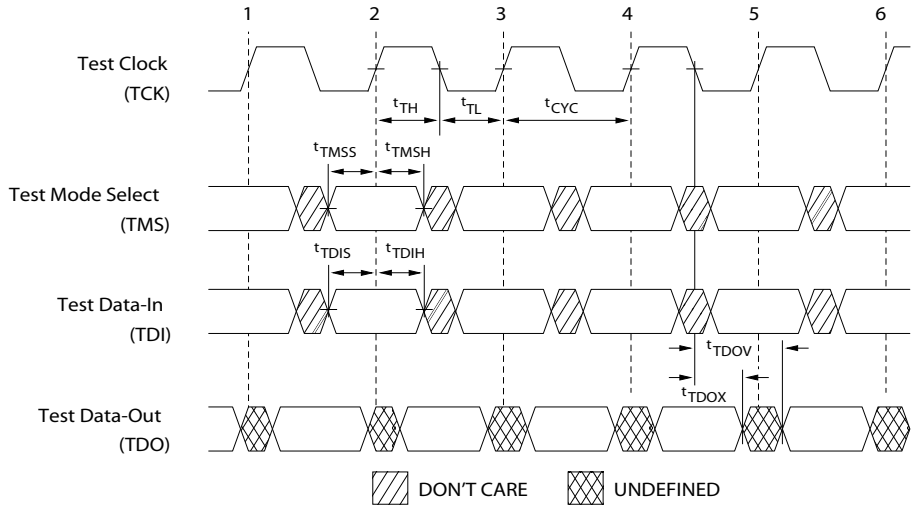


The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing Diagram



[+] Feedback

TAP AC Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH time	20	–	ns
t_{TL}	TCK clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns

Notes
13. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
14. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

[+] Feedback

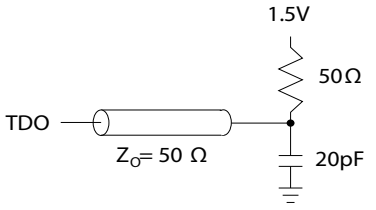
3.3 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 3.3 V
Input rise and fall times ..... 1 ns
Input timing reference levels ..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

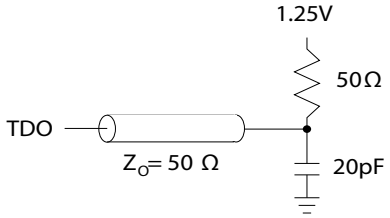
2.5 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter[15]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 8.0 mA, V_{DDQ} = 3.3 V		–	0.4	V
		I_{OL} = 8.0 mA, V_{DDQ} = 2.5 V		–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH voltage	V_{DDQ} = 3.3 V		2.0	V_{DD} + 0.3	V
		V_{DDQ} = 2.5 V		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage	V_{DDQ} = 3.3 V		–0.5	0.7	V
		V_{DDQ} = 2.5 V		–0.3	0.7	V
I_X	Input load current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
15. All voltages referenced to V_{SS} (GND).

[+] Feedback

Identification Register Definitions

Instruction Field	CY7C1386D/CY7C1386F (512 K × 36)	CY7C1387D/CY7C1387F (1 M × 18)	Description
Revision Number (31:29)	000	000	Describes the version number
Device Depth (28:24) [16]	01011	01011	Reserved for internal use.
Device Width (23:18) 119-ball BGA	101110	101110	Defines the memory type and architecture.
Device Width (23:18) 165-ball FBGA	000110	000110	Defines the memory type and architecture.
Cypress Device ID (17:12)	100101	010101	Defines the width and density.
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 18)	Bit Size (× 36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	85	85
Boundary Scan Order (165-ball FBGA package)	89	89

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note
16. Bit #24 is 1 in the register definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

119-ball BGA [17, 18]

Bit #	Ball ID
1	H4
2	T4
3	T5
4	T6
5	R5
6	L5
7	R6
8	U6
9	R7
10	T7
11	P6
12	N7
13	M6
14	L7
15	K6
16	P7
17	N6
18	L6
19	K7
20	J5
21	H6
22	G7

Bit #	Ball ID
23	F6
24	E7
25	D7
26	H7
27	G6
28	E6
29	D6
30	C7
31	B7
32	C6
33	A6
34	C5
35	B5
36	G5
37	B6
38	D4
39	B4
40	F4
41	M4
42	A5
43	K4
44	E4

Bit #	Ball ID
45	G4
46	A4
47	G3
48	C3
49	B2
50	B3
51	A3
52	C2
53	A2
54	B1
55	C1
56	D2
57	E1
58	F2
59	G1
60	H2
61	D1
62	E2
63	G2
64	H1
65	J3
66	2K

Bit #	Ball ID
67	L1
68	M2
69	N1
70	P1
71	K1
72	L2
73	N2
74	P2
75	R3
76	T1
77	R1
78	T2
79	L3
80	R2
81	T3
82	L4
83	N4
84	P4
85	Internal

Notes
17. Balls that are NC (No Connect) are preset LOW.
18. Bit#85 is preset HIGH.

[+] Feedback

Boundary Scan Order

165-ball BGA [19, 20]

Bit #	Ball ID
1	N6
2	N7
3	N10
4	P11
5	P8
6	R8
7	R9
8	P9
9	P10
10	R10
11	R11
12	H11
13	N11
14	M11
15	L11
16	K11
17	J11
18	M10
19	L10
20	K10
21	J10
22	H9
23	H10
24	G11
25	F11
26	E11
27	D11
28	G10
29	F10
30	E10

Bit #	Ball ID
31	D10
32	C11
33	A11
34	B11
35	A10
36	B10
37	A9
38	B9
39	C10
40	A8
41	B8
42	A7
43	B7
44	B6
45	A6
46	B5
47	A5
48	A4
49	B4
50	B3
51	A3
52	A2
53	B2
54	C2
55	B1
56	A1
57	C1
58	D1
59	E1
60	F1

Bit #	Ball ID
61	G1
62	D2
63	E2
64	F2
65	G2
66	H1
67	H3
68	J1
69	K1
70	L1
71	M1
72	J2
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Notes
19. Balls that are NC (No Connect) are preset LOW.
20. Bit#89 is preset HIGH.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ..... –0.5 V to +V_{DD}

DC voltage applied to outputs in tristate .....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) .....> 2001 V

Latch-up current .....> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / +10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	361	394	FIT/ Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Electrical Characteristics

Over the Operating Range

Parameter [21, 22]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage		3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage [21]	for 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage [21]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled	–5	5	µA

Notes
21. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5 V (pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > –2$ V (pulse width less than $t_{CYC}/2$).
22. $T_{Power\text{-}up}$: assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

[+] Feedback

Electrical Characteristics (continued)

Over the Operating Range

Parameter [21, 22]	Description	Test Conditions		Min	Max	Unit
I_{DD}	V_{DD} operating supply current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz	–	350	mA
			5 ns cycle, 200 MHz	–	300	mA
			6 ns cycle, 167 MHz	–	275	mA
I_{SB1}	Automatic CE power-down current—TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz	–	160	mA
			5 ns cycle, 200 MHz	–	150	mA
			6 ns cycle, 167 MHz	–	140	mA
I_{SB2}	Automatic CE power-down current—CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0	All speeds	–	70	mA
I_{SB3}	Automatic CE power-down current—CMOS inputs	V_{DD} = Max, device deselected, or $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz	–	135	mA
			5 ns cycle, 200 MHz	–	130	mA
			6 ns cycle, 167 MHz	–	125	mA
I_{SB4}	Automatic CE power-down current—TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speeds	–	80	mA

Capacitance

Parameter[23]	Description	Test Conditions	100-pin TQFP Max	119-ball BGA Max	165-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	8	9	pF
C_{CLK}	Clock input capacitance		5	8	9	pF
C_{IO}	I/O capacitance		5	8	9	pF

Thermal Resistance

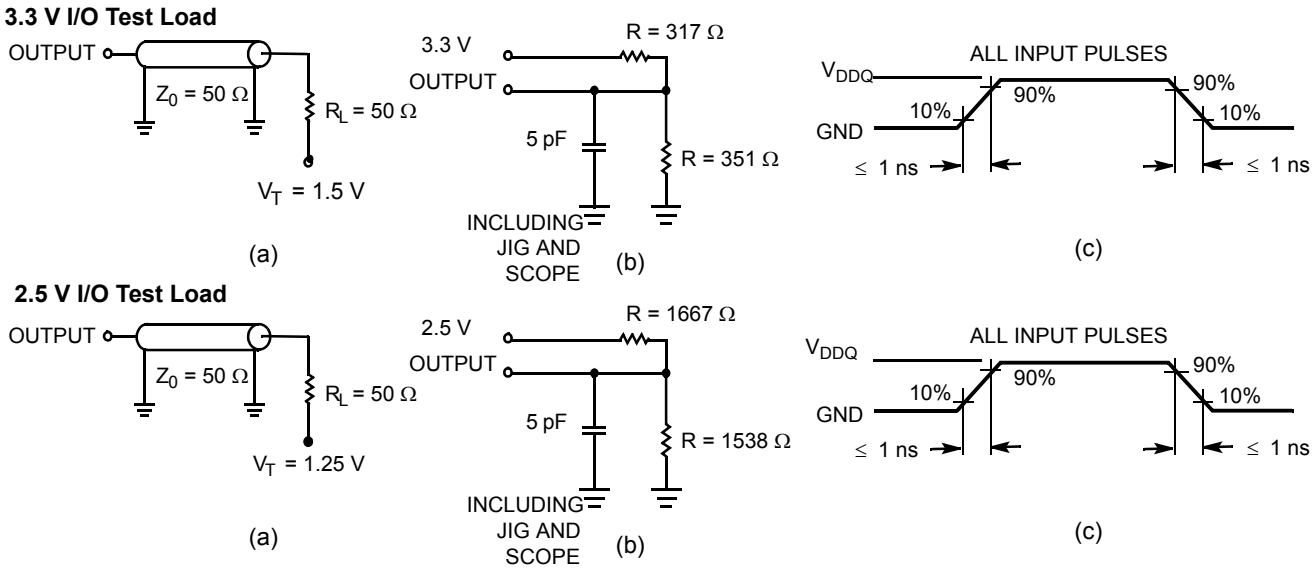
Parameter[23]	Description	Test Conditions	100-pin TQFP Package	119-ball BGA Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.66	23.8	20.7	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.08	6.2	4.0	°C/W

Note
23. Tested initially and after any design or process change that may affect these parameters.

[+] Feedback

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



[+] Feedback

Switching Characteristics

Over the Operating Range

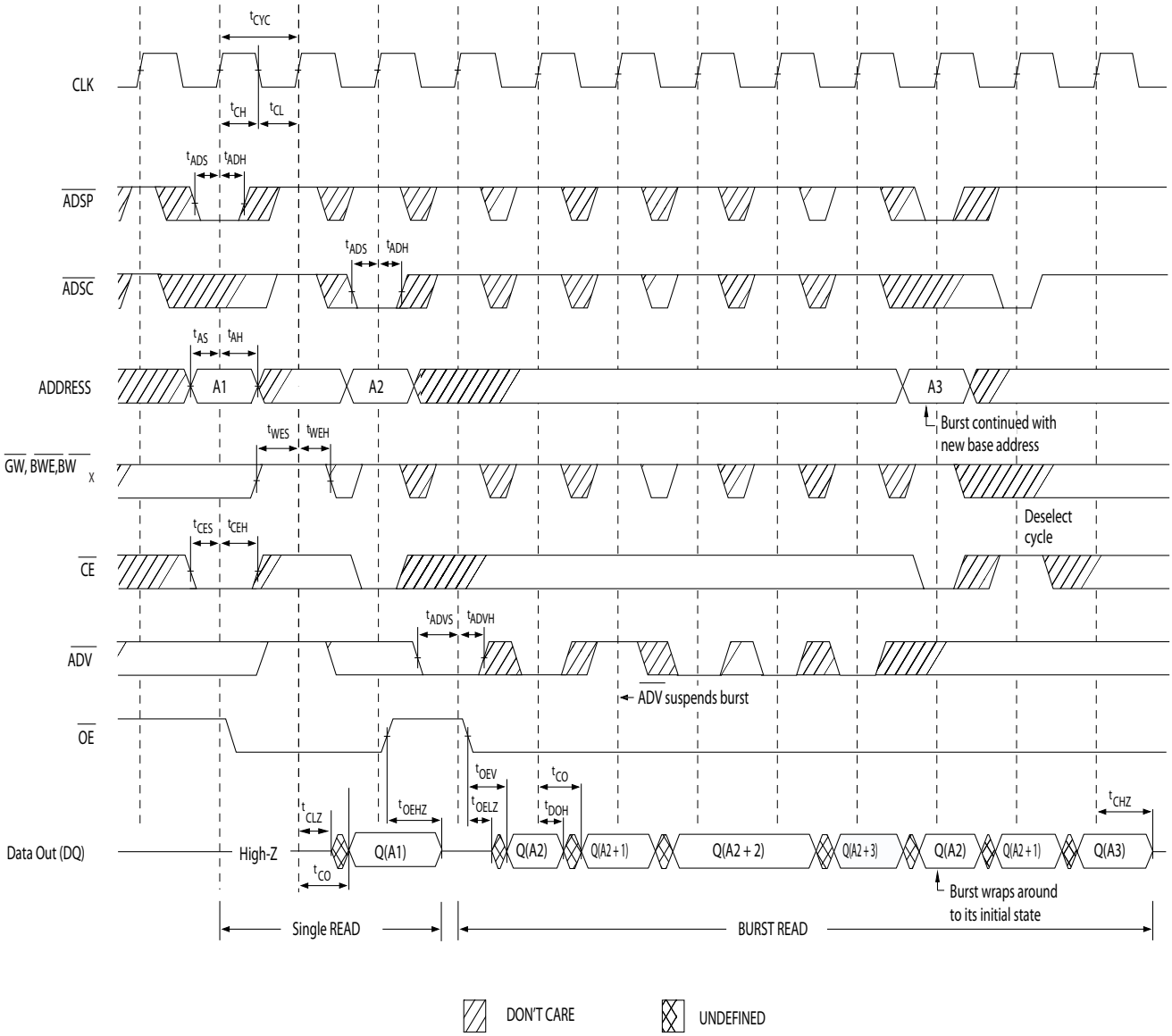
Parameter [24, 25]	Description	-250		-200		-167		Unit
		Min	Max	Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first access [26]	1	–	1	–	1	–	ms
Clock								
t_{CYC}	Clock cycle time	4.0	–	5.0	–	6.0	–	ns
t_{CH}	Clock HIGH	1.7	–	2.0	–	2.2	–	ns
t_{CL}	Clock LOW	1.7	–	2.0	–	2.2	–	ns
Output Times								
t_{CO}	Data output valid after CLK rise	–	2.6	–	3.0	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.0	–	1.3	–	1.3	–	ns
t_{CLZ}	Clock to low Z [27, 28, 29]	1.0	–	1.3	–	1.3	–	ns
t_{CHZ}	Clock to high Z [27, 28, 29]	–	2.6	–	3.0	–	3.4	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	2.6	–	3.0	–	3.4	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [27, 28, 29]	0	–	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [27, 28, 29]	–	2.6	–	3.0	–	3.4	ns
Setup Times								
t_{AS}	Address setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{CES}	Chip enable setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
Hold Times								
t_{AH}	Address hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.3	–	0.4	–	0.5	–	ns

Notes
24. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
25. Test conditions shown in (a) of Figure 4 on page 23 unless otherwise noted.
26. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation can be initiated.
27. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in (b) of Figure 4 on page 23. Transition is measured ±200 mV from steady-state voltage.
28. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
29. This parameter is sampled and not 100% tested.

[+] Feedback

Switching Waveforms

Figure 5. Read Cycle Timing [30]

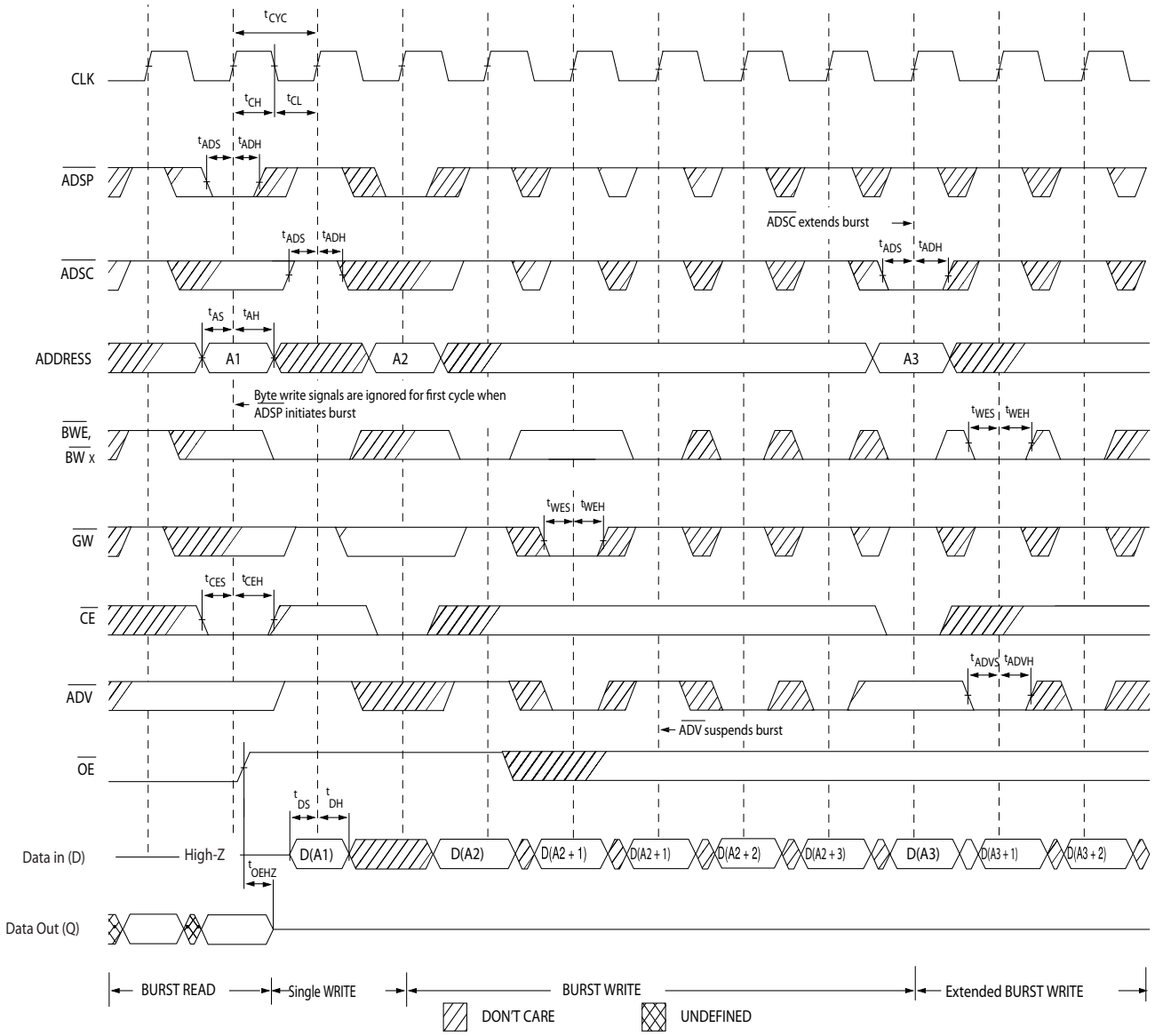


Note
30. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

[+] Feedback

Switching Waveforms (continued)

Figure 6. Write Cycle Timing [31]

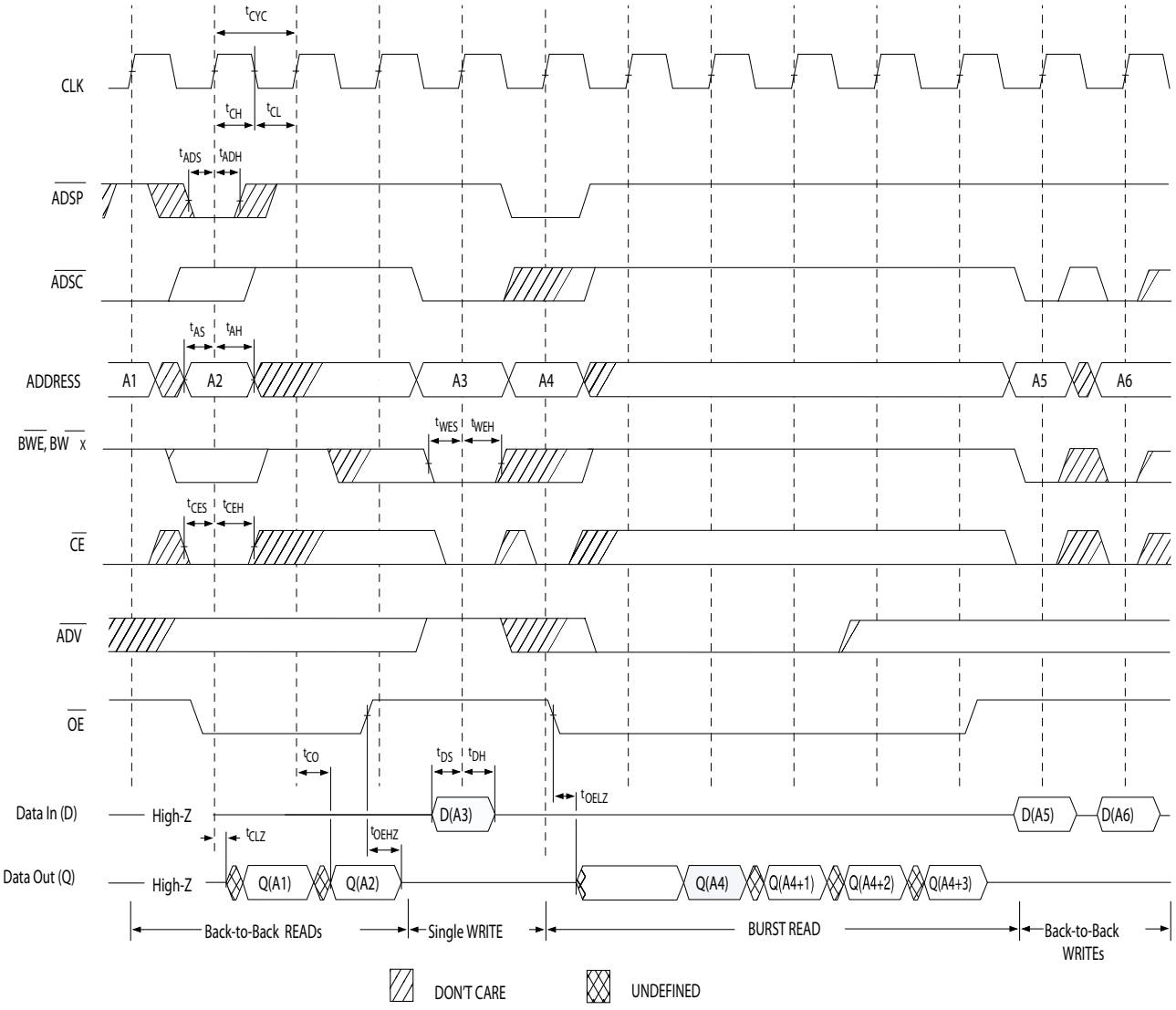


Note
31. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

[+] Feedback

Switching Waveforms (continued)

Figure 7. Read/Write Cycle Timing [32, 33, 34]

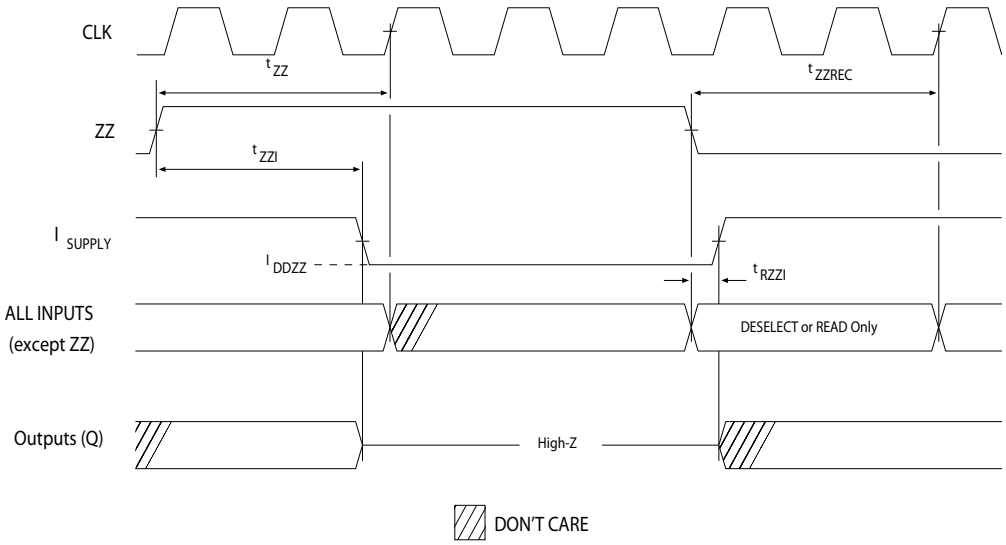


Notes
32. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.
33. The data bus (Q) remains in high Z following a Write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
34. $\overline{GW}$ is HIGH.

[+] Feedback

Switching Waveforms (continued)

Figure 8. ZZ Mode Timing [35, 36]



Notes
35. Device must be deselected when entering ZZ sleep mode. See cycle descriptions table for all possible signal conditions to deselect the device.
36. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

The table below contains only the parts that are currently available. If you do not see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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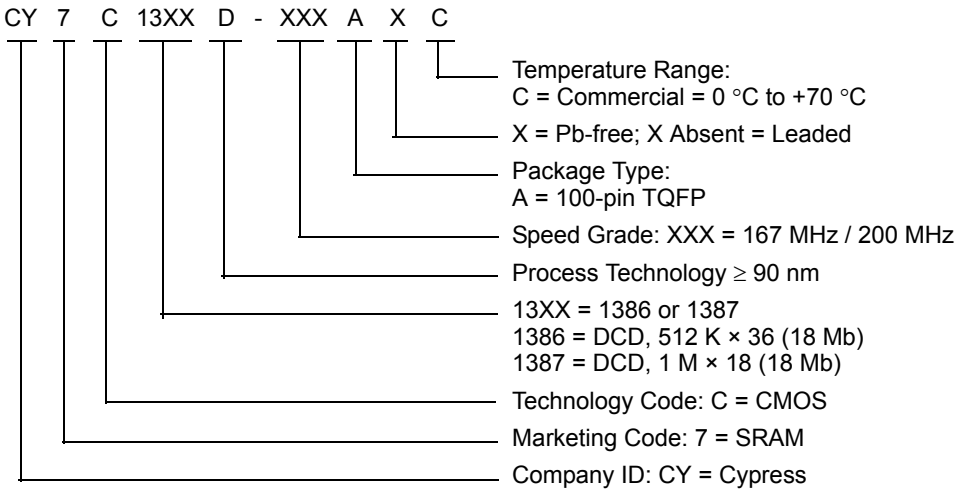
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1386D-167AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1387D-167AXC			
200	CY7C1386D-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

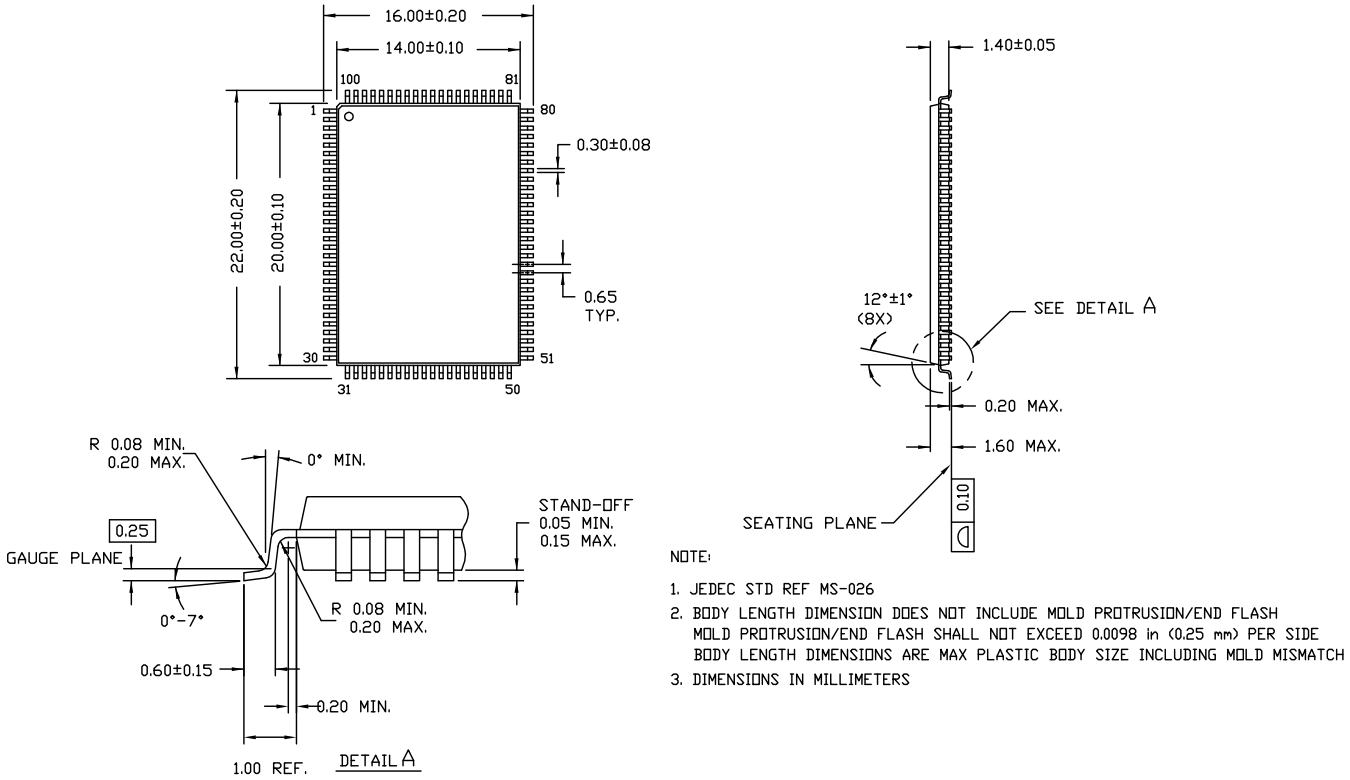
Ordering Code Definitions


CY 7 C 13XX D - XXX A X C
Temperature Range:
C = Commercial = 0 °C to +70 °C
X = Pb-free; X Absent = Leaded
Package Type:
A = 100-pin TQFP
Speed Grade: XXX = 167 MHz / 200 MHz
Process Technology ≥ 90 nm
13XX = 1386 or 1387
1386 = DCD, 512 K × 36 (18 Mb)
1387 = DCD, 1 M × 18 (18 Mb)
Technology Code: C = CMOS
Marketing Code: 7 = SRAM
Company ID: CY = Cypress

[+] Feedback

Package Diagrams

Figure 10: 100-pin TQFP (14 × 20 × 1.4 mm) A100RA, 51-85050



NOTE:

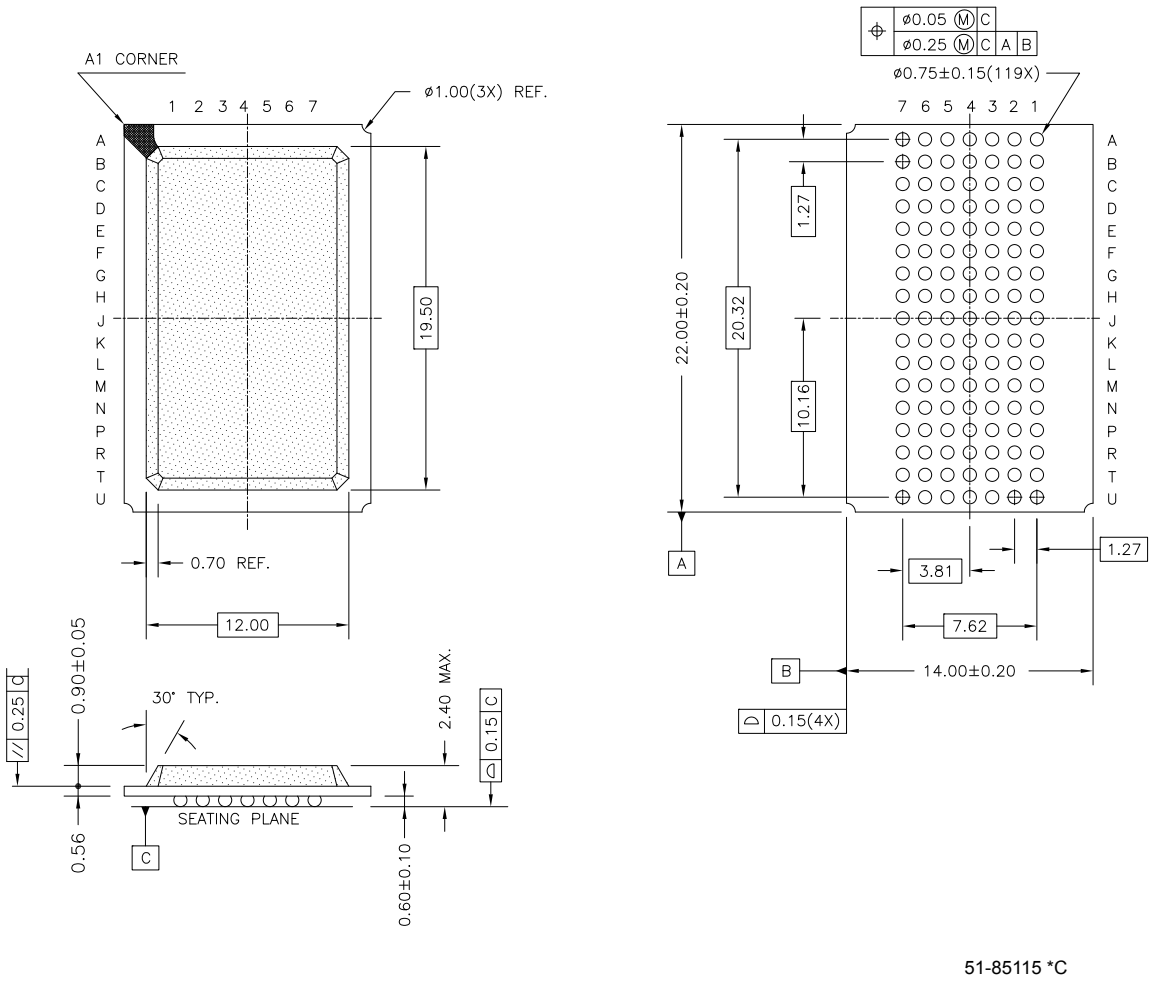
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

[+] Feedback

Package Diagrams (continued)

Figure 9. 119-ball PBGA (14 × 22 × 2.4 mm) BG119, 51-85115

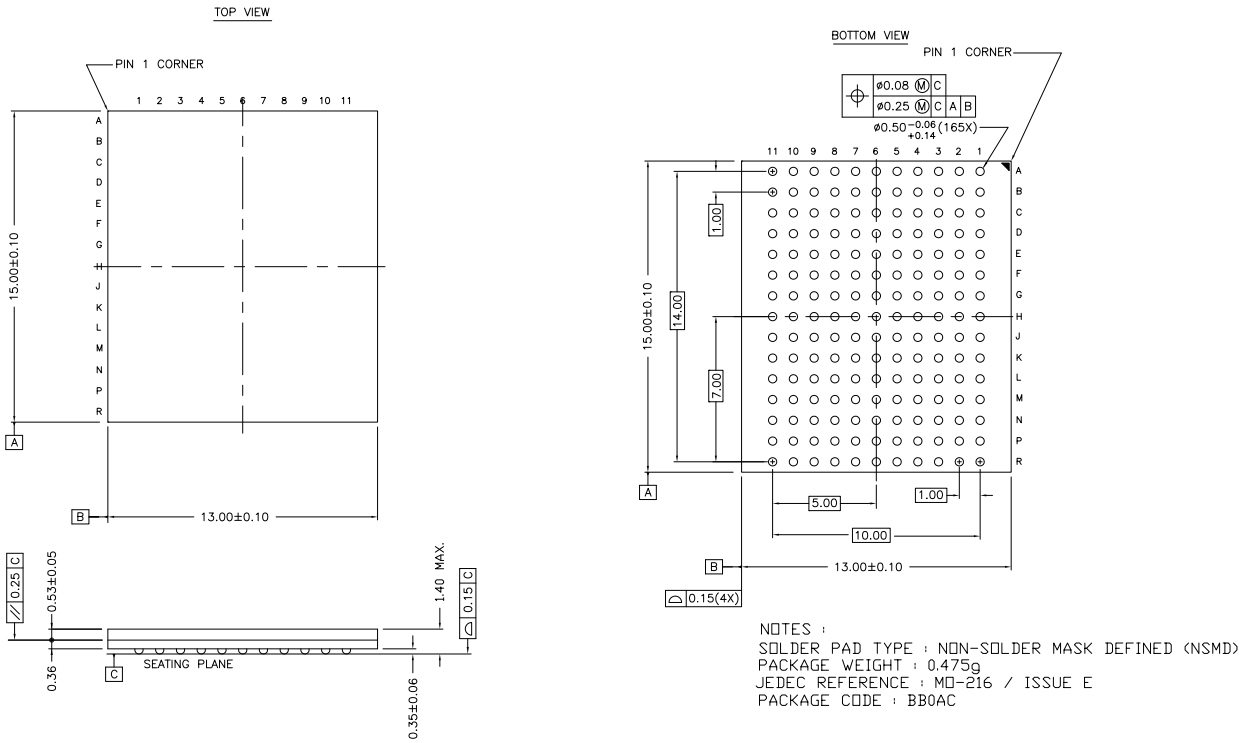


51-85115 *C

[+] Feedback

Package Diagrams (continued)

Figure 10. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter), 51-85180



51-85180 *C

[+] Feedback

Acronyms

Acronym	Description
BGA	ball grid array
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
FBGA	fine-pitch ball grid array
I/O	input/output
JTAG	Joint Test Action Group
LMBU	logical multiple-bit upsets
LSB	least significant bit
LSBU	logical single-bit upsets
MSB	most significant bit
$\overline{OE}$	output enable
SEL	single event latch-up
SRAM	static random access memory
TAP	test access port
TCK	test clock
TDI	test data-in
TDO	test data-out
TMS	test mode select
TQFP	thin quad flat pack
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilo ohms
MHz	Mega Hertz
µA	micro Amperes
µs	micro seconds
mA	milli Amperes
mV	milli Volts
mm	milli meter
ms	milli seconds
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts

Document History Page

Document Title: CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F, 18-Mbit (512 K × 36/1 M × 18) Pipelined DCD Sync SRAM Document Number: 38-05545				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	254550	RKF	See ECN	New data sheet
*A	288531	SYT	See ECN	Edited description under “IEEE 1149.1 Serial Boundary Scan (JTAG)” for non-compliance with 1149.1 Removed 225 MHz Speed Bin Added Pb-free information for 100-pin TQFP, 119 BGA and 165 FBGA Packages. Added comment of ‘Pb-free BG packages availability’ below the Ordering Information
*B	326078	PCI	See ECN	Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added description on EXTEST Output Bus Tristate Changed description on the Tap Instruction Set Overview and Extest Changed Device Width (23:18) for 119-BGA from 000110 to 101110 Added separate row for 165 -FBGA Device Width (23:18) Changed Θ_{JA} and Θ_{JC} for TQFP Package from 31 and 6 °C/W to 28.66 and 4.08 °C/W respectively Changed Θ_{JA} and Θ_{JC} for BGA Package from 45 and 7 °C/W to 23.8 and 6.2 °C/W respectively Changed Θ_{JA} and Θ_{JC} for FBGA Package from 46 and 3 °C/W to 20.7 and 4.0 °C/W respectively Modified V_{OL}, V_{OH} test conditions Removed comment of ‘Pb-free BG packages availability’ below the Ordering Information Updated Ordering Information Table
*C	418125	NXR	See ECN	Converted from Preliminary to Final. Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed the description of I_X from Input Load Current to Input Leakage Current on page# 18. Changed the I_X current values of MODE on page # 18 from –5 μA and 30 μA to –30 μA and 5 μA. Changed the I_X current values of ZZ on page # 18 from –30 μA and 5 μA to –5 μA and 30 μA. Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$on page # 18. Replaced Package Name column with Package Diagram in the Ordering Information table. Updated Ordering Information Table.
*D	475009	VKN	See ECN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*E	793579	VKN	See ECN	Added Part numbers CY7C1386F and CY7C1387F Added footnote# 3 regarding Chip Enable Updated Ordering Information table
*F	2756940	VKN	08/27/2009	Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information.
*G	3006369	NJY	08/12/10	Template update. Added Ordering Code Definitions. Added Acronyms.

[+] Feedback

Document History Page (continued)

Document Title: CY7C1386D/CY7C1387D/CY7C1386F/CY7C1387F, 18-Mbit (512 K × 36/1 M × 18) Pipelined DCD Sync SRAM Document Number: 38-05545				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	3309506	OSN	07/12/2011	Updated Package Diagrams. Added Units of Measure. Updated in new template.

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